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10/561,135	04/25/2006	Martin Vorbach	2885/98	9404

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,135	VORBACH ET AL.	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 12-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 12-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to amendments received on 12/10/2008.

2. Claims 1-7 and 12-30 presented for examination. Claims 8-11 cancelled.

3. Applicant's replacements of drawing, specification and abstract have been considered and entered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-7 and 12-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. As per claim 1, the claim recites "*the unit is operable independently of….",* there is insufficient antecedent basis for "*the unit"* in the claim. It should be changed to "*the at least one unit"*. Furthermore, claim 1 recites "*an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and a configurable network",* this limitation appears to be indefinite. It's not clear whether the configurable network belongs to the array or part of the data processing cells. Appropriate correction/clarification is required.

7. As per claim 2, the claim recites "*transferring via at least one data path at least one an input and an output between the at least one unit and the array",* it's not clear what's been transferred. As well known in the art, input and output are usually ports, thus, it's not clear how a port is transferred. Perhaps the applicant meant "input data" and "output data". Appropriate correction is required.

Furthermore, claim 2 recites "*and comprising at least one FIFO so as to allow for at least one of a coupling between and a data processing within at least one unit and the array that is not strictly synchronous*", this limitation appears to be indefinite. The way it's written is vague and unclear, for instance it says "between and a data….", a feature after the word between appears to be missing. Also, "within the at least one unit and the array that is not strictly synchronous appears to be vague with relationship to the previous features in the claim. Appropriate correction/clarification is required.

8. As per claim 3, the recites *"wherein the transferring is performed by at least one of inserting data directly into and extracting data directly from a data path of at least one of the at least one unit and the array*", the current claim language is vague and unclear. It appears that there is a structure to perform the transferring, however, in the claim it's referring to a step of inserting and extracting. Also, the last feature of the claim is vague as currently written.

9. As per claim 5, the claim recites "*the unit is operable independently of….",* there is insufficient antecedent basis for "*the unit"* in the claim. It should be changed to "*the at least one unit".*

10. As per claim 6, the claim recites "*the unit….",* there is insufficient antecedent basis for "*the unit"* in the claim. It should be changed to "*the at least one unit".* Furthermore, claim 6 recites "*coupling between and a data processing within the at least one unit and the array that is not strictly synchronous"* this limitation appears to be indefinite. The way it's written is vague and unclear, for instance it says "between and a data….", a feature after the word between appears to be missing. Also, "within the at least one unit and the array that is not strictly synchronous appears to be vague with relationship to the previous features in the claim. Appropriate correction/clarification is required.

11. As per claim 7, the claim recites "*an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and a configurable network",* this limitation appears to be indefinite. It's not clear whether the configurable network belongs to the array or part of the data processing cells. Appropriate correction/clarification is required.

12. As per claim 26, the claim recites "*coupling between and a data processing within the at least one unit and the array that is not strictly synchronous"* this limitation

appears to be indefinite. The way it's written is vague and unclear, for instance it says "between and a data....", a feature after the word between appears to be missing. Also, "within the at least one unit and the array that is not strictly synchronous appears to be vague with relationship to the previous features in the claim. Appropriate correction/clarification is required.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-7 and 12-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Dawes U.S. Patent No. 4,967,340 (hereinafter Dawes)

15. As per claim 1, Dawes teaches a method of processing data comprising the step of:

coupling:

(a) at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline (see Fig. 2, element 48); and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and a configurable network (see Fig. 2, elements 28, 50 and abstract);

wherein:

the unit is operable independently of the array (see Fig. 2, element 48, which operates independent of the array processor element 28); and

the array is:

at least one of coarse grained and runtime reconfigurable (see abstract and col. 1, line 65 to col. 2, line 12); and

coupled into the instruction pipeline (see Fig. 2, wherein element 48 is coupled into element 28 “array processor”).

16. As per claim 2, Dawes further teaches a method according to claim 1, further comprising the step of:

transferring via at least one data path at least one of the an input and an output between the at least one unit and the array, the at least one data path being provided therebetween and comprising at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not strictly synchronous (see abstract and col. 5, lines 27-64).

17. As per claim 3, Dawes further teaches a method according to claim 2, wherein the transferring is performed by at least one of inserting data directly into and extracting data directly from a data path of at least one of the at least one unit and the array (see col. 5, lines 40-64).

18. As per claim 4, Dawes further teaches a method according to claim 3, further comprising the step of:

providing between the at least one unit and the array a path adapted for transfer of at least one of status information and event information (see col. 5, lines 40-64; see also Fig. 2, communications between element 48 and 28).

19. As per claim 5, Dawes teaches a device for processing data comprising:

at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline (see Fig. 2, element 48); and

an array adapted for processing data comprising a configurable network and a plurality of data processing cells that are configurable in their function (see Fig. 2, elements 28, 50 and abstract);

wherein:

the array is coupled into the instruction pipeline (see Fig. 2, wherein element 48 is coupled into element 28 “array processor”); and

the unit is operable independently of the array (see Fig. 2, element 48, which operates independent of the array processor element 28).

20. As per claim 6, Dawes further teaches the device according to claim 5, wherein at least one of:

at least one data path is provided between the array and the unit, the at least one data path comprising at least one FIFO that allows at least one of a coupling between

and a data processing within the at least one unit and the array that is not strictly synchronous (see abstract and col. 5, lines 27-64); and

data is transferred by at least one of extracting data directly from and inserting data directly into a data path of at least one of the at least one unit and the array (col. 5, lines 40-64).

21. As per claim 7, Dawes further teaches a method of processing data comprising the steps of:

coupling:

(a) at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline (see Fig. 2, element 48); and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and a configurable network (see Fig. 2, elements 28, 50 and abstract); and

providing a path allowing for block data transfer from the array and at least one of a data cache and another data source (see abstract and col. 2, lines 2-31).

22. As per claim 12, Dawes further teaches a method according to claim 1, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller (Fig. 2, element 48).

23. As per claim 13, Dawes further teaches a method according to claim 1, wherein the array includes at least one of a data processor, a Field Programmable Gate-Array (FPGA), a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric (see abstract and Fig. 2, elements 28 and 50).

24. As per claim 14, Dawes further teaches a method according to claim 2, wherein the at least one data path between the at least one unit and the array includes at least one local memory connected to the at least one unit as a cache and connected to the array (see Fig. 2 and col. 2, lines 2-45).

25. As per claim 15, Dawes further teaches a method according to claim 14, wherein the at least one local memory includes an internal RAM (IRAM) (see col. 2, lines 12-24).

26. As per claim 16, Dawes further teaches a method according to claim 1, wherein configuration information for the array is issued by the instruction pipeline of the at least one unit (see abstract and col. 5, lines 27-64).

27. As per claim 17, Dawes further teaches a method according to claim 16, further comprising:

buffering the configuration information in at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not strictly synchronous (see col. 5, lines 27-64).

28. As per claim 18, Dawes further teaches a method according to claim 1, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit (see col. 5, lines 27-64).

29. As per claim 19, Dawes further teaches a method according to claim 18, wherein the array is operable synchronously to the unit (see abstract and col. 5, lines 27-64).

30. As per claim 20, Dawes further teaches a method according to claim 4, wherein the at least one of the status information and the event information includes at least one of flags, an overflow, and a carry (see col. 2, lines 1-61).

31. As per claim 21, Dawes further teaches a device according to claim 5, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller (see Fig. 2, element 48).

32. As per claim 22, Dawes further teaches a device according to claim 5, wherein the array includes at least one of (a) a runtime and reconfigurable data processor, (b) a Data Flow Processor (DFP), (c) a Digital Signal Processor (DSP), (d) an extreme

Processing Platform (XPP), and (e) a chaemeleon-technology data processing fabric (see abstract and col. 2, lines 2-24).

33. As per claim 23, Dawes further teaches a device according to claim 6, wherein the at least one data path includes at least one local memory connected to the unit as cache and connected to the array (see abstract and col. 5, lines 27-64).

34. As per claim 24, Dawes further teaches a method according to claim 23, wherein the at least one local memory includes an internal RAM (IRAM) (see col. 2, lines 12-24).

35. As per claim 25, Dawes further teaches a device according to claim 5, wherein configuration information for the array is issued by the instruction pipeline (see abstract and col. 5, lines 27-64).

36. As per claim 26, Dawes further teaches a device according to claim 25, wherein the configuration information is buffered in at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not strictly synchronous (see abstract and col. 5, lines 27-64).

37. As per claim 27, Dawes further teaches a device according to claim 5, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit (see col. 5, lines 27-64).

38. As per claim 28, Dawes further teaches a device according to claim 27, wherein the array operates synchronously to the unit (see abstract and col. 5, lines 27-64).

39. As per claim 29, Dawes further teaches a method according to claim 7, wherein the at least one unit includes at least one of a CPU, a von-Neumann-processor, and a microcontroller (Fig. 2, element 48 and abstract).

40. As per claim 30, Dawes further teaches a method according to claim 7, wherein the array includes at least one of a runtime and reconfigurable data processor, a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric (see abstract and Fig. 2, elements 28 and 50).

Response to Arguments

41. Applicant's arguments with respect to claims have been considered but are moot in view of the new grounds of rejection.

Conclusion

42. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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